

111RK SERIES

Power Silicon Controlled Rectifiers

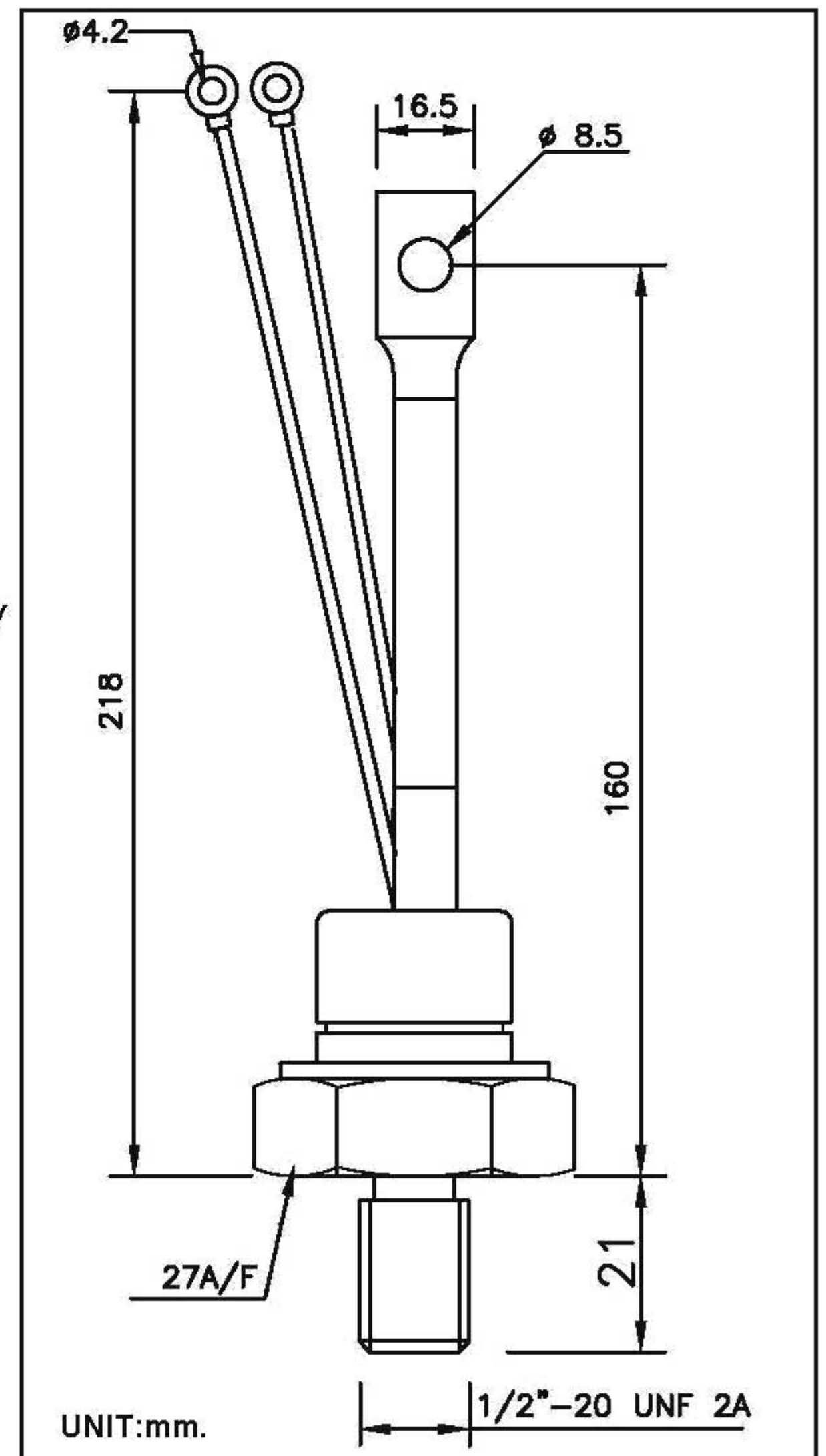
Types : 111RK10 TO 111RK160

FEATURES

- ❖ All diffused series.
- ❖ International Standard Case TO-209 AC (TO-94).
- ❖ Threaded studs UNF 1/2" - 20 UNF 2A.
- ❖ High di/dt and dv/dt capabilities.
- ❖ Reliable blocking at elevated temperature.
- ❖ High surge current rating 2700 A.
- ❖ High I²t capability 36400 A²Sec.
- ❖ Excellent dynamic characteristics.
- ❖ Compression Bonded Encapsulation for heavy duty operations such as severe thermal cycling.

THERMAL MECHANICAL SPECIFICATIONS

R _{thjc}	Maximum thermal resistance junction to case	0.20K/W
R _{thcs}	Contact thermal resistance case-to-sink	0.08K/W
T _j	Junction operating temp. range	-40°C to +125°C
T _{stg}	Storage temperature range	-40°C to +150°C
	Mounting torque (Non-lubricated threads)	14.0Nm. Min. 15.5Nm. Max.
	Approximate weight	130 gms.



ELECTRICAL RATINGS

TYPE	111RK	10	20	40	60	80	100	120	140	160
V _{DRM}	Max. repetitive peak off state voltage (V)	100	200	400	600	800	1000	1200	1400	1600
V _{RRM}	Max. repetitive peak reverse voltage (V)	100	200	400	600	800	1000	1200	1400	1600
V _{RSM}	Max. non-repetitive peak reverse voltage (V)	150	300	500	700	900	1100	1300	1500	1700
I _{RM} & I _{DM}	Max. peak reverse & off state current @ rated V _{DRM} & V _{RRM} 125°C -mA	20	20	20	20	20	20	20	20	20

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ELECTRICAL SPECIFICATION ON-STATE CONDITION

	Parameter	111RK	Units	Conditions
$I_{T(AV)}$	Max. average on-state current @ case temperature	110	A	180°C conduction, half sine wave
		90	°C	
$I_{T(RMS)}$	Max. RMS on-state current	175		
I_{TSM}	Max. peak one cycle non-repetitive surge current	2270	A	t = 10ms
I^2t	Maximum I^2t for fusing	25.76	kA ² s	t = 10ms
$V_{T(TO)}$	Threshold voltage	0.90	V	$T_J = T_J \text{ max.}$
r_t	On state slope resistance	1.79	mΩ	$T_J = T_J \text{ max.}$
V_{TM}	Max. on state voltage	1.52	V	$I_{pk} = 350A, T_J = 125°C, t_p = 10ms$ sine pulse
I_H	Maximum holding current	300	mA	$T_J = 25°C$, anode supply 12V resistive load
I_L	Latching current	600		

TRIGGERING

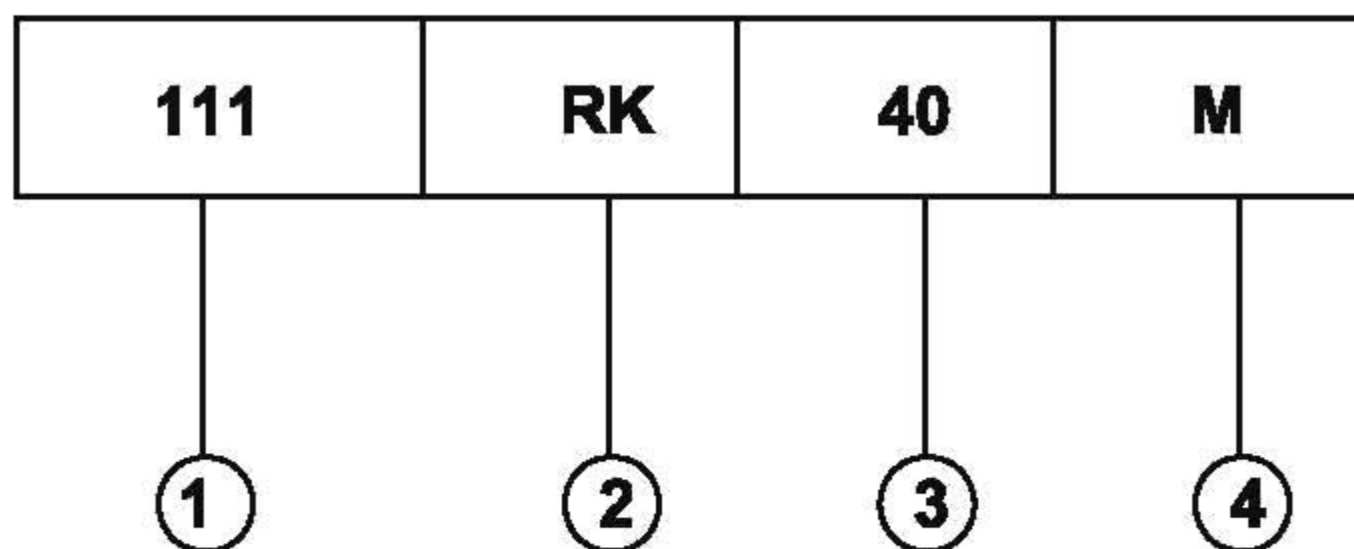
	Parameter	111RK	Units	Conditions
P_{GM}	Maximum peak gate power	5	W	$T_J = 125°C, t_p \leq 5ms$
$P_{G(AV)}$	Maximum average gate power	1		$T_J = 125°C, f = 50Hz, d\% = 50$
I_{GM}	Max. peak positive gate current	2.0	A	$T_J = 125°C, t_p \leq 5ms$
$+V_{GM}$	Max. peak positive gate voltage	20	V	$T_J = 125°C, t_p \leq 5ms$
$-V_{GM}$	Max. peak negative gate voltage	5.0		
I_{GT}	DC gate current required to trigger	Typ.	Max.	$T_J = 25°C$
		90	150	
V_{GT}	DC gate voltage required to trigger	1.8	3.0	$T_J = 25°C$
I_{GD}	DC gate current not to trigger	10	mA	$T_J = 125°C$
V_{GD}	DC gate voltage not to trigger	0.25		

Max. required gate trigger / current / voltage are the lowest value which will trigger all units 12V anode-to-cathode applied.

Max. gate current / voltage not to trigger is the max. value which will not trigger any unit with rated V_{DRM} anode-to-cathode applied.

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ORDER INFORMATION TABLE



- ① - Current Code
- ② - RK - Essential part number
- ③ - Voltage Rating (See table)
- ④ - None - Stud 1/2" 20UNF 2A Threading
M - Stud M16 x 1.5P Metric Threading

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Switching

Parameter	111RK	Unit	Condition
di/dt Max. non-repetitive rate of rise of turned-on current	100	A/μs	Gate drive 20V, 20Ω, tr ≤ 1μs T _J -125°C, anode voltage < 80% V _{DRM}
t _d Typical delay time	2.0	μs	Gate current 1A, di/dt -1A/μs V _d -0.67% V _{DRM} , T _J -25°C
t _q Typical turn-off time	100	μs	I _{TM} -100A, T _J -125°C, di/dt- 10A/μs, V _r -50V dv/dt -20V/μs, Gate 0v 100Ω, t _p - 500μs

Blocking

Parameter	111RK	Unit	Condition
dv/dt Max. critical rate of rise of off-state voltage	500	V/μs	T _J -125°C, Linear to 80% rated V _{DRM}
I _{RRM} / I _{DRM} Max. peak reverse and off-stage leakage current	20	mA	T _J -125°C, rated V _{DRM} / V _{RRM} applied

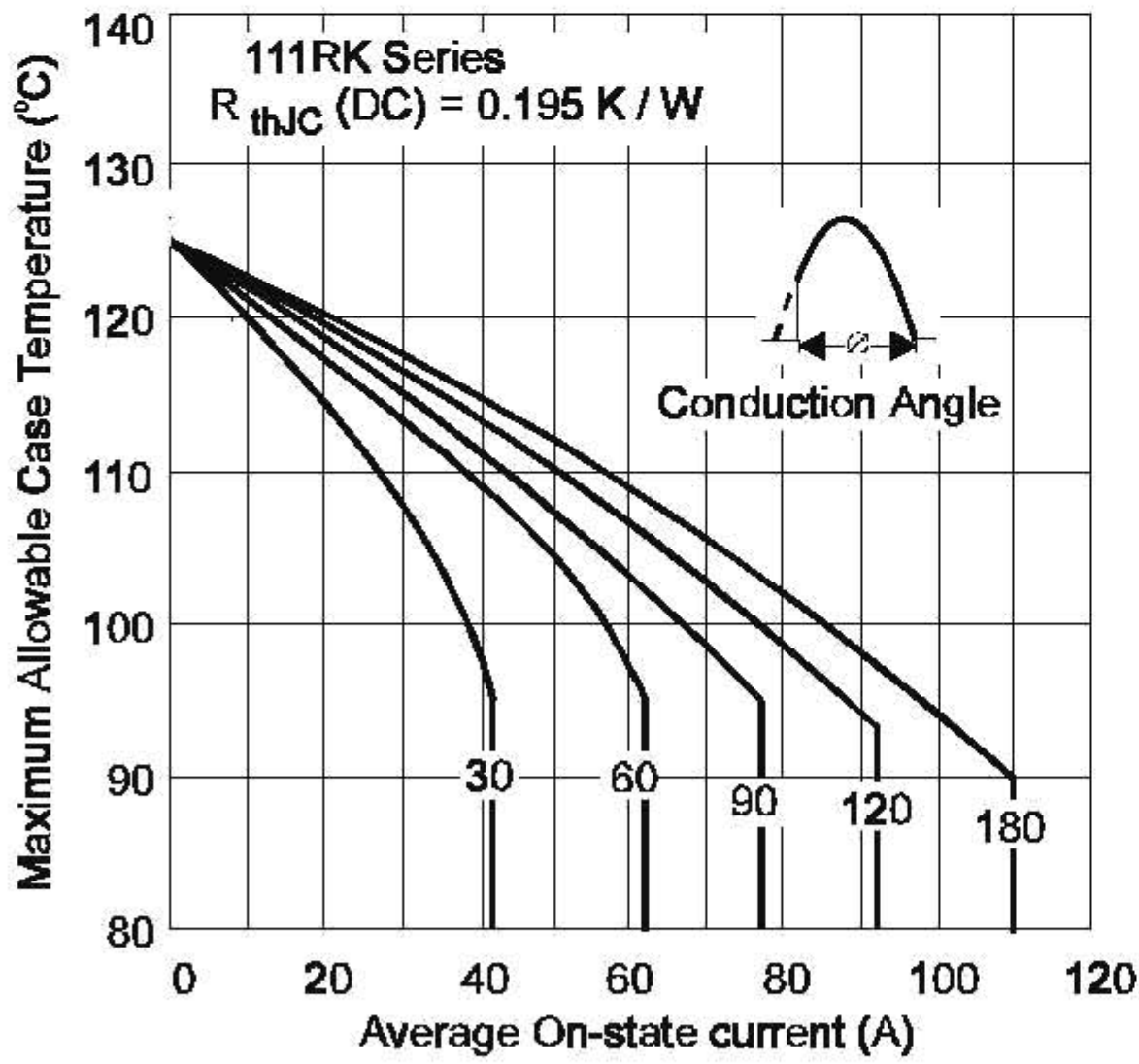


Fig. 1 - Current Ratings Characteristics

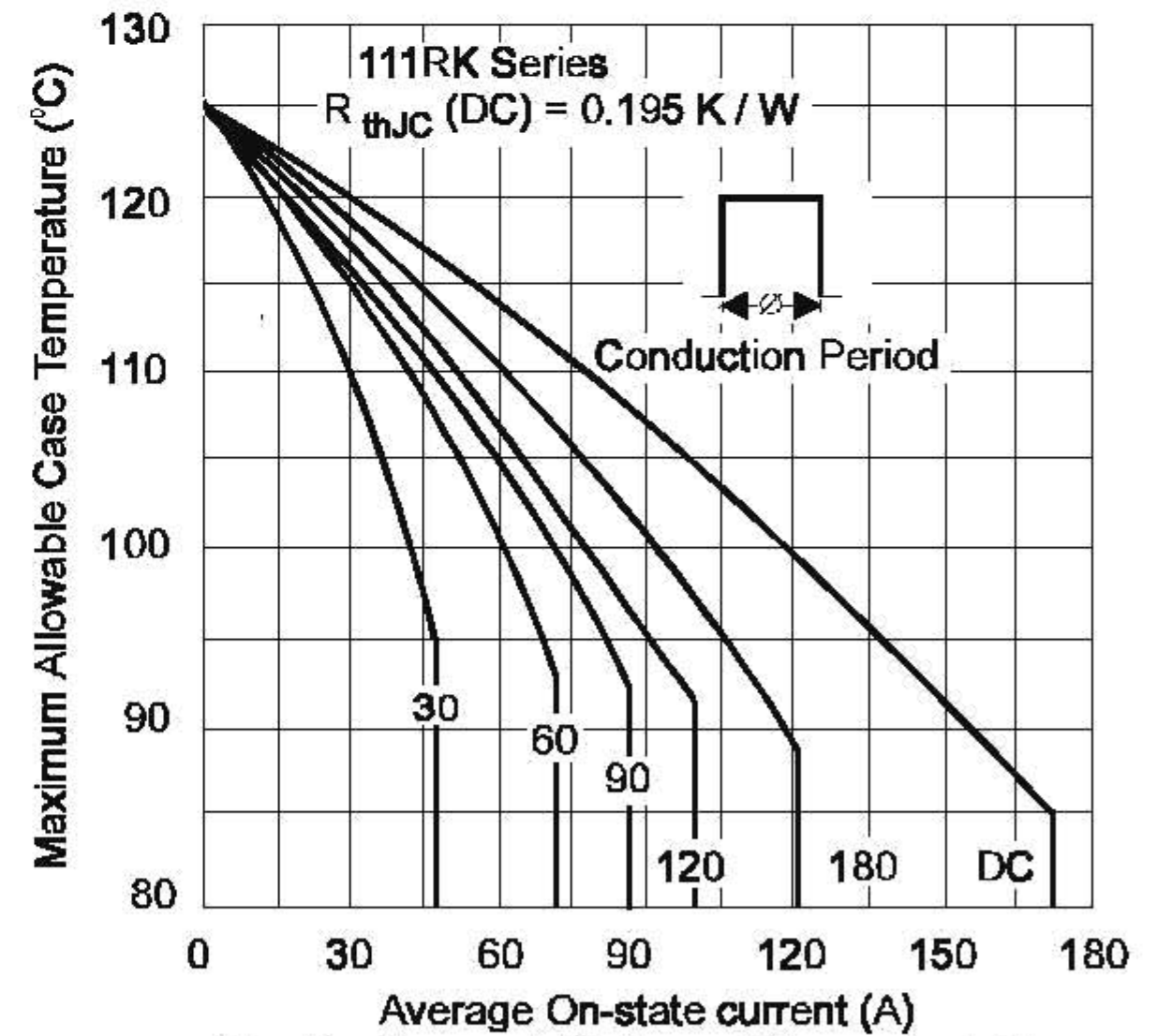


Fig. 2 - Current Ratings Characteristics

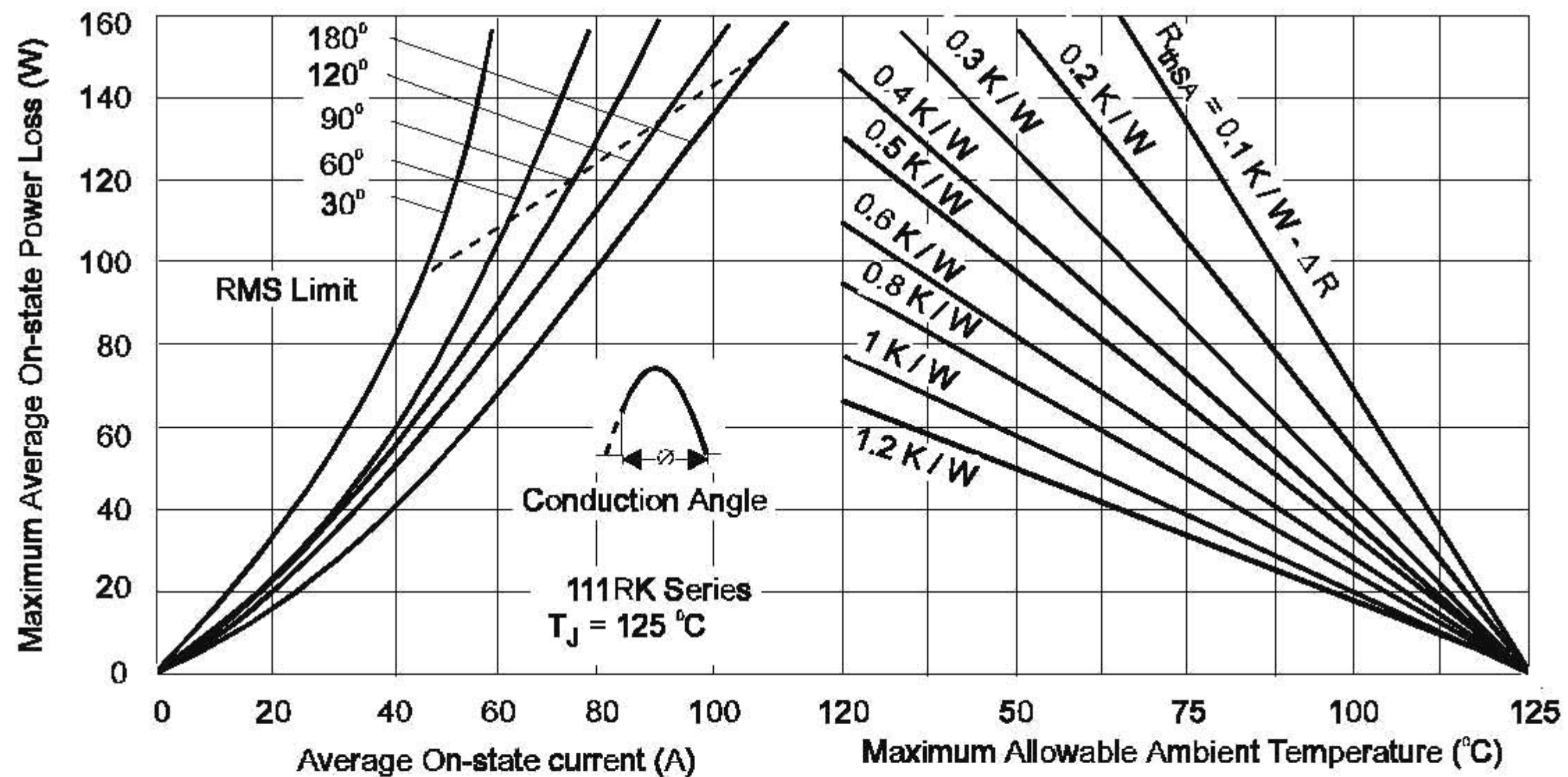
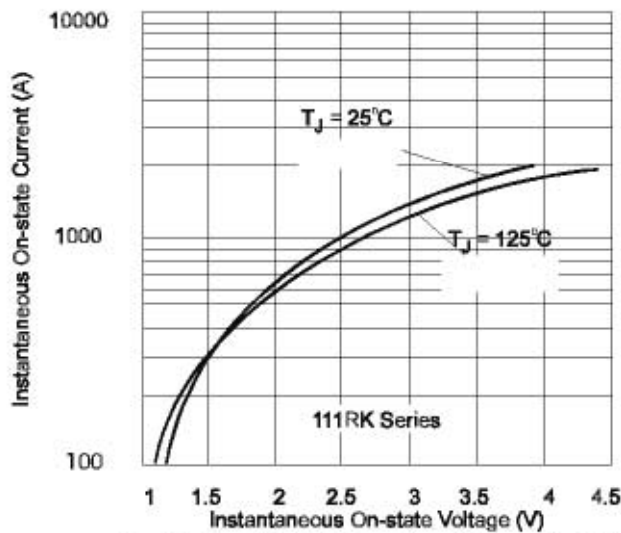
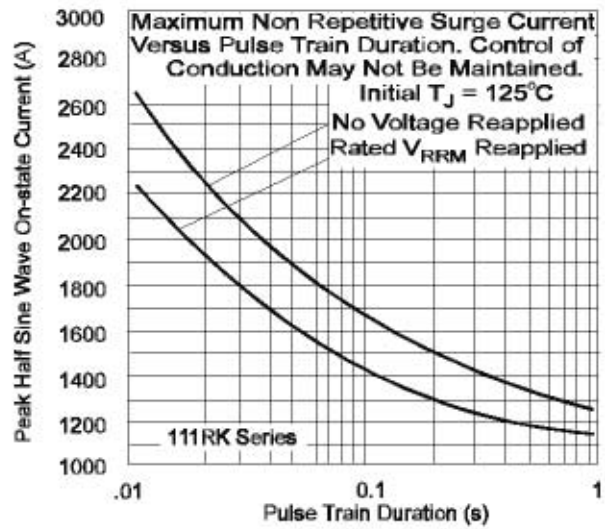
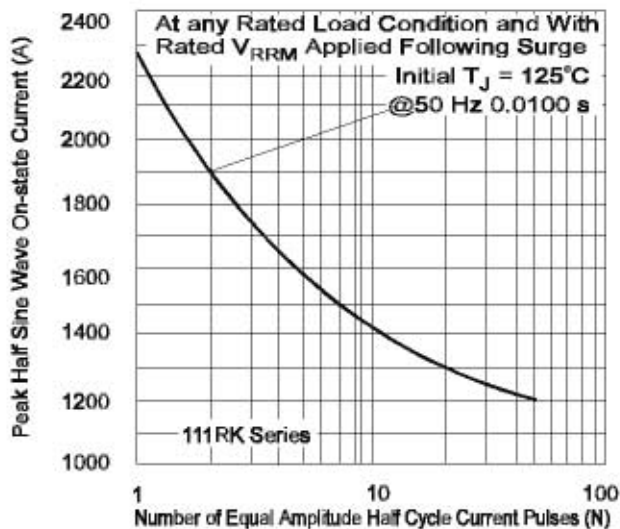
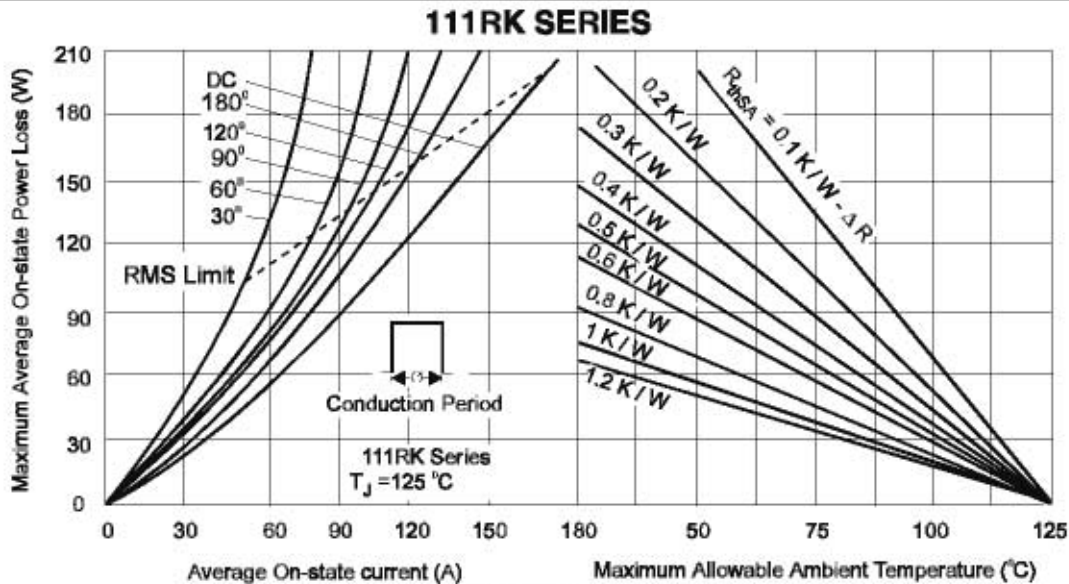


Fig. 3 - On-state Power Loss Characteristics

SILICON CONTROLLED RECTIFIERS



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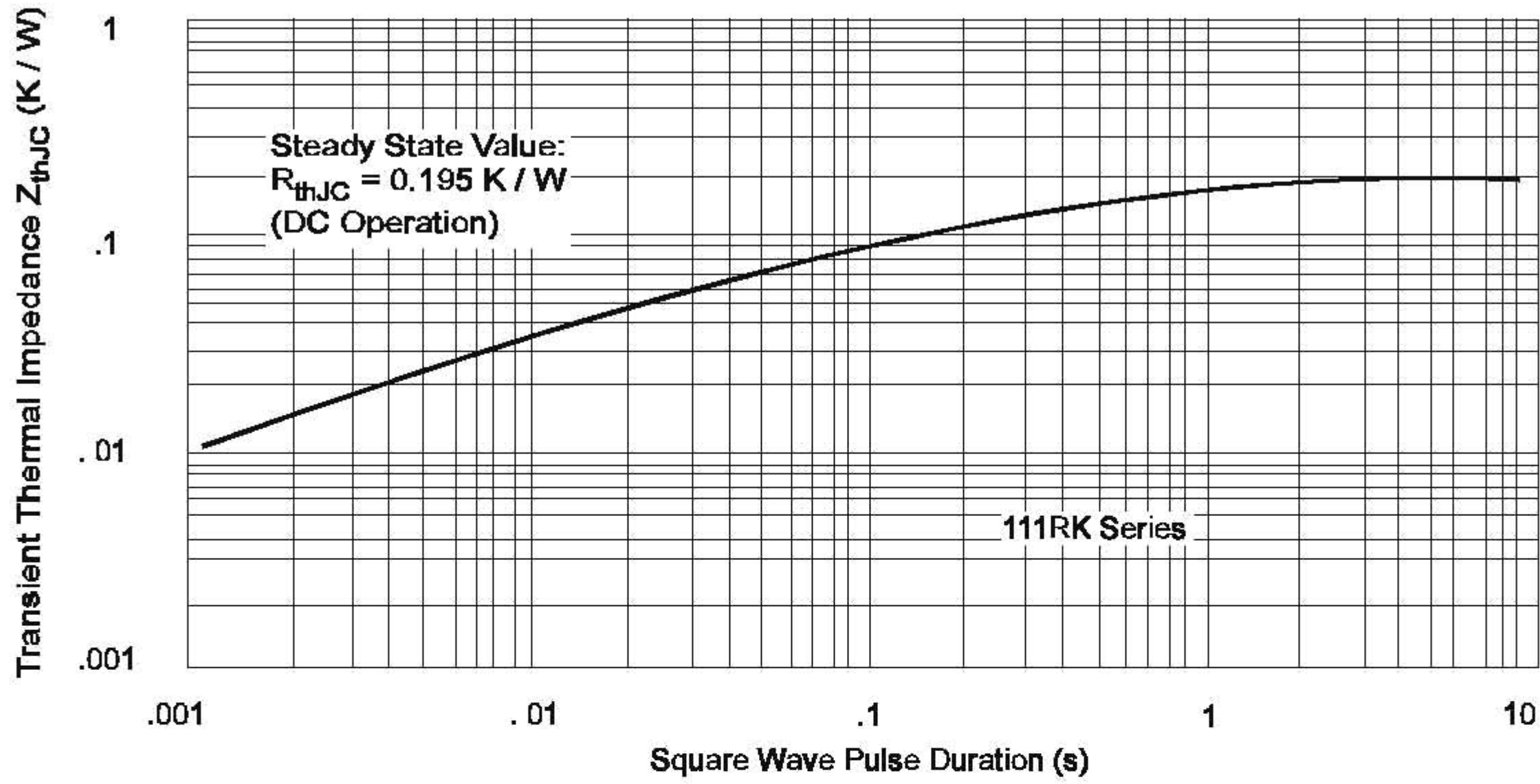


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

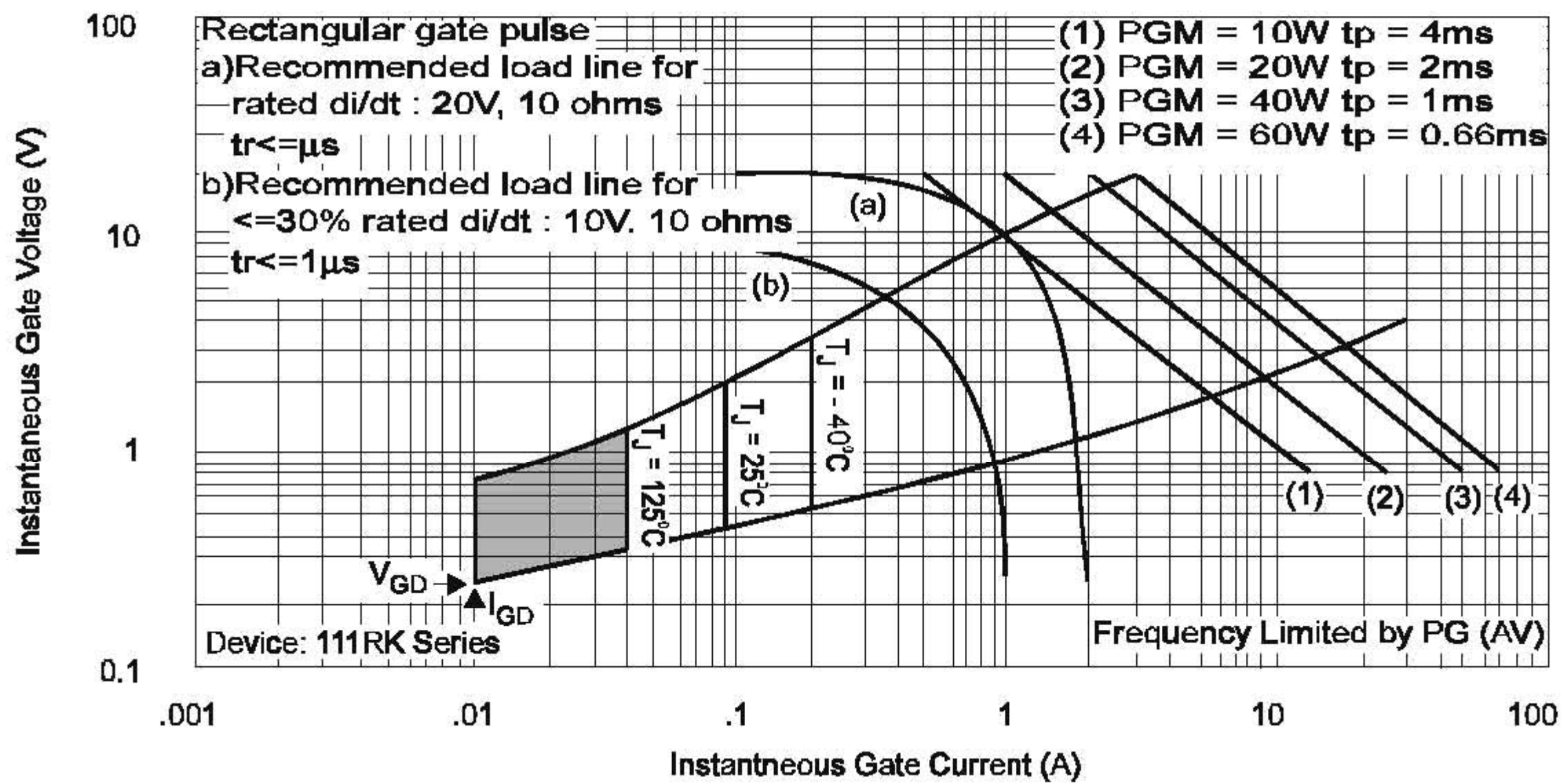


Fig. 9 - Gate Characteristics